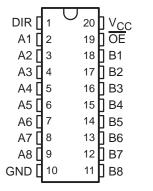
SCES275G - JUNE 1999 - REVISED AUGUST 2003

- Operates From 2.7 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 6.3 ns at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V<sub>CC</sub>)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## DB, DW, N, NS, OR PW PACKAGE (TOP VIEW)



#### description/ordering information

This octal bus transceiver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCZ245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so the buses are effectively isolated.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

#### **ORDERING INFORMATION**

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 20	SN74LVCZ245AN	SN74LVCZ245AN
	SOIC - DW	Tube of 25	SN74LVCZ245ADW	LVCZ245A
	SOIC - DW	Reel of 2000	SN74LVCZ245ADWR	LVCZZ43A
4000 to 0500	SOP - NS	Reel of 2000	SN74LVCZ245ANSR	LVCZ245A
–40°C to 85°C	SSOP – DB	Reel of 2000	SN74LVCZ245ADBR	CV245A
		Tube of 70	SN74LVCZ245APW	CV245A
	TSSOP – PW	Reel of 2000	SN74LVCZ245APWR	CV245A
		Reel of 250	SN74LVCZ245APWT	CV245A

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



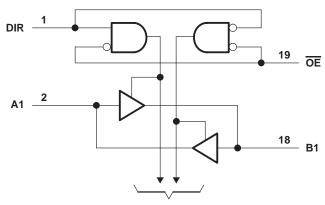
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#### **FUNCTION TABLE**

INP	UTS	OPERATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

#### logic diagram (positive logic)



To Seven Other Channels

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		
Voltage range applied to any output in the high	-impedance or power-off state, VO	
(see Note 1)		–0.5 V t0 6.5 V
(see Notes 1 and 2)		1.000000000000000000000000000000000000
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through V <sub>CC</sub> or GND		±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3)	: DB package	70°C/W
	DW package	58°C/W
	N package	89°C/W
	NS package	60°C/W
	PW package	83°C/W
Storage temperature range, T <sub>stg</sub>		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage V	CC = 2.7 V to 3.6 V	2		V
V <sub>IL</sub>	Low-level input voltage V	CC = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	5.5	V
Va	Output voltage	ligh or low state	0	Vcc	V
۷o	Output voltage 3-	3-state		5.5	V
la	Visib lovel output output	CC = 2.7 V		-12	mA
ЮН	High-level output current	CC = 3 V		-24	IIIA
la.	V <sub>1</sub>	CC = 2.7 V		12	mA
lOL	Low-level output current	CC = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate			6	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		150		μs/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	ARAMETER	TEST CONDIT	IONS	VCC	MIN	TYP <sup>†</sup>	MAX	UNIT
		I <sub>OH</sub> = -100 μA		2.7 V to 3.6 V	V <sub>CC</sub> -0.2			
\/-··		10 mA		2.7 V	2.2			V
VOH		$I_{OH} = -12 \text{ mA}$		3 V	2.4			V
		I <sub>OH</sub> = -24 mA		3 V	2.2			
		I <sub>OL</sub> = 100 μA		2.7 V to 3.6 V			0.2	
VOL		I <sub>OL</sub> = 12 mA	2.7 V			0.4	V	
		I <sub>OL</sub> = 24 mA	3 V			0.55		
ΙĮ	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μΑ	
l <sub>off</sub>	-	V <sub>I</sub> or V <sub>O</sub> = 5.5 V		0			±5	μΑ
loz‡		V <sub>O</sub> = 0 to 5.5 V		3.6 V			±5	μΑ
lozpu		$V_0 = 0.5 \text{ V to } 2.5 \text{ V},$	OE = don't care	0 to 1.5 V			±5	μΑ
lozpd		$V_0 = 0.5 \text{ V to } 2.5 \text{ V},$	OE = don't care	1.5 V to 0			±5	μΑ
		V <sub>I</sub> = V <sub>CC</sub> or GND		2.6.1/			100	A
ICC 3.6 '		$3.6 \text{ V} \le \text{V}_1 \le 5.5 \text{ V}$ $I_0 = 0$		3.6 V			100	μΑ
∆lcc	$\Delta I_{CC}$ One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GI		inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			100	μΑ
Ci	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		4		pF
Cio	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		6		pF	



<sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C. ‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>§</sup> This applies in the disabled state only.

#### SN74LVCZ245A OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

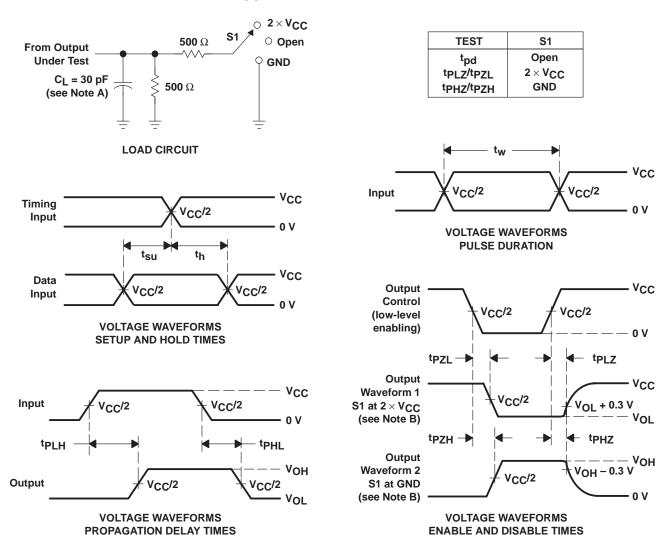
PARAMETER	FROM	FROM TO (OUTPUT) –				UNIT
	(1141 01)	(0011 01)	MIN MAX	MIN	MAX	
<sup>t</sup> pd	A or B	B or A	7.3	1.5	6.3	ns
t <sub>en</sub>	ŌĒ	A or B	9.5	1.5	8.5	ns
<sup>t</sup> dis	ŌĒ	A or B	8.5	1.7	7.5	ns

## operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 3.3 V TYP	UNIT	
Card	Power discipation conscitance per transceiver	Outputs enabled	f = 10 MHz	42	pF
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	I = IO WIHZ	3	pΓ



## PARAMETER MEASUREMENT INFORMATION $V_{CC}$ = 2.7 V AND 3.3 V $\pm$ 0.3 V



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 2$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpl 7 and tpH7 are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







4-Jun-2007

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVCZ245ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LVCZ245ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LVCZ245ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ245APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs. **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.



#### PACKAGE OPTION ADDENDUM

4-Jun-2007

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

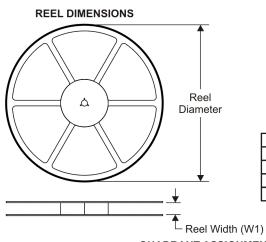
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCZ245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCZ245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVCZ245ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVCZ245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCZ245ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LVCZ245ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LVCZ245ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LVCZ245APWR	TSSOP	PW	20	2000	346.0	346.0	33.0

#### DB (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

#### PW (R-PDSO-G\*\*)

#### 14 PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

#### **MECHANICAL DATA**

#### NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## DW (R-PDSO-G20)

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



## N (R-PDIP-T\*\*)

#### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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